Amendments to the Specification:

(All references to page and line refer to the Substitute Specification included with the Response mailed June 13, 2003.)

Please replace the paragraph beginning on line 16 of page 6 with the following amended paragraph:

Fig. 3B shows details of a typical register used to select a sector for erase as shown in Fig. ~~2A~~ 3A;

Please replace the paragraph beginning on line 10 of page 9 with the following amended paragraph:

The EEprom array 33 includes a number of EEprom integrated circuit chips 43, 45, 47, etc. Each includes a respective chip select and enable line 49, 51 and 53 from interface circuits 40. The interface circuits 40 also act to interface between the serial data lines 35, 37 and a circuit [[23]] 57. Memory location addresses and data being written into or read from the EEprom chips 43, 45, 47, etc. are communicated from a bus 55, through logic and register circuits 57 and thence by another bus 59 to each of the memory chips 43, 45, 47 etc.